AMENDMENTS TO THE CLAIMS

1. (Original) A printed circuit board (PCB) structure usable in a connector for reducing crosstalk, the PCB structure comprising:

at least one PCB, the PCB including a plurality of substrates and a plurality of metalized layers between the substrates, the substrates including at least one first substrate made of a first material and at least one second substrate made of a second material, the first material having a first dielectric constant, the second material having a second dielectric constant lower in rate of decline with frequency than the first dielectric constant;

at least one first capacitor provided on the at least one first substrate at a first stage area of the PCB structure; and

at least one second capacitor provided on the at least one second substrate at a second stage area of the PCB structure.

2. (Original) The PCB structure of claim 1, wherein the first dielectric constant is about 4.0 at 1MHz with a rate of decline being 0.4 per decade of frequency between 1MHz and 1GHz.

3. (Original) The PCB structure of claim 1, wherein the second dielectric constant is about 4.0 and remains constant across a frequency range of 1MHz and 1GHz.

4. (Original) The PCB structure of claim 1, wherein the substrates of the PCB are five substrates stacked on each other,

a first one, a second one, and a portion of a third one of the substrates are made of the second material, and

a portion of the third one, a fourth one, and a fifth one of the substrates are made of the first material.

5. (Original) The PCB structure of claim 4, wherein the at least one first capacitor includes two first capacitor components formed on the fourth one and fifth one of the substrates at the first stage area of the PCB structure.

6. (Original) The PCB structure of claim 5, wherein the two first capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

7. (Original) The PCB structure of claim 4, wherein the at least one second capacitor includes two second capacitor components formed on the second one and third one of the substrates at the second stage area of the PCB structure.

8. (Original) The PCB structure of claim 7, wherein the two second capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

9. (Original) The PCB structure of claim 1, wherein the substrates of the PCB are four substrates stacked on each other,

a first one and a second one of the substrates are made of the first material, and

a third one and a fourth one of the substrates are made of the second material.

10. (Original) The PCB structure of claim 9, wherein the at least one first capacitor includes a first capacitor formed on the second one of the substrates at the first stage area of the PCB structure.

11. (Original) The PCB structure of claim 9, wherein the at least one second capacitor includes a second capacitor formed on the fourth one of the substrates at the second stage area of the PCB structure.

12. (Original) The PCB structure of claim 1, wherein the at least one PCB includes first and second PCBs, the first PCB including substrates made of the first material, the second PCB including substrates made of the second material.

13. (Original) The PCB structure of claim 12, wherein the at least one first capacitor includes two first capacitor components formed on at least two of the substrates of the first PCB at the first stage area of the PCB structure.

14. (Original) The PCB structure of claim 13, wherein the two first capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

15. (Original) The PCB structure of claim 12, wherein the at least one second capacitor includes two second capacitor components formed on at least two of the substrates of the second PCB at the second stage area of the PCB structure.

16. (Original) The PCB structure of claim 15, wherein the two second capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

17. (Original) A printed circuit board (PCB) structure usable in a connector for reducing crosstalk, the PCB structure comprising:

a printed circuit board (PCB) including a plurality of substrates stacked up and a plurality of metalized layers between the substrates, the substrates being made of a material with a dielectric constant having a high rate of decline with frequency;

at least one first capacitor provided on one of the substrates at a first stage area of the PCB structure; and

at least one second capacitor provided on one of the substrates at a second stage area of the PCB structure.

18. (Original) The PCB structure of claim 17, wherein the substrate material has a dielectric constant of about 4.0 at 1MHz with a rate of decline being 0.4 per decade of frequency between 1MHz and 1GHz.

19. (Original) The PCB structure of claim 17, wherein the at least one first capacitor includes two first capacitor components formed on at least two of the substrates at the first stage area of the PCB structure.

20. (Original) The PCB structure of claim 19, wherein the two first capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

21. (Original) The PCB structure of claim 17, wherein the at least one second capacitor includes a separate second discreet capacitor surface-mounted on a first one or under a last one of the substrates at the second stage area of the PCB structure.

22. (Original) A connector for reducing crosstalk, comprising:

at least one printed circuit board (PCB), the PCB including a plurality of substrates and a plurality of metalized layers between the substrates, the substrates including at least one first substrate made of a first material and at least one second substrate made of a second material, the first material having a first dielectric constant, the second material having a second dielectric constant lower in rate of decline with frequency than the first dielectric constant;

at least one first capacitor provided on the at least one first substrate at a first stage area of the connector;

at least one second capacitor provided on the at least one second substrate at a second stage area of the connector; and

at least one conductive contact provided on the PCB.

23. (Original) The connector of claim 22, wherein the first dielectric constant is about 4.0 at 1MHz with a rate of decline being 0.4 per decade of frequency between 1MHz and 1GHz.

24. (Original) The connector of claim 22, wherein the second dielectric constant is about 4.0 and remains constant across a frequency range of 1MHz and 1GHz.

25. (Original) The connector of claim 22, wherein the substrates of the PCB are five substrates stacked on each other,

a first one, a second one, and a portion of a third one of the substrates are made of the second material, and

a portion of the third one, a fourth one, and a fifth one of the substrates are made of the first material.

26. (Original) The connector of claim 25, wherein the at least one first capacitor includes two first capacitor components formed on the fourth one and fifth one of the substrates at the first stage area of the connector.

27. (Original) The connector of claim 25, wherein the at least one second capacitor includes two second capacitor components formed on the second one and third one of the substrates at the second stage area of the connector.

28. (Original) The connector of claim 22, wherein the substrates of the PCB are four substrates stacked on each other,

a first one and a second one of the substrates are made of the first material, and

a third one and a fourth one of the substrates are made of the second material.

29. (Original) The connector of claim 28, wherein the at least one first capacitor includes a first capacitor formed on the second one of the substrates at the first stage area of the connector.

30. (Original) The connector of claim 28, wherein the at least one second capacitor includes a second capacitor formed on the fourth one of the substrates at the second stage area of the connector.

31. (Original) The connector of claim 22, wherein the at least one PCB includes first and second PCBs, the first PCB including substrates made of the first material, the second PCB including substrates made of the second material.

32. (Original) The connector of claim 31, wherein the at least one first capacitor includes two first capacitor components formed on at least two of the substrates of the first PCB at the first stage area of the connector.

33. (Original) The connector of claim 31, wherein the at least one second capacitor includes two second capacitor components formed on at least two of the substrates of the second PCB at the second stage area of the connector.

34. (Original) A connector for reducing crosstalk, comprising:

a printed circuit board (PCB) including a plurality of substrates stacked up and a plurality of metalized layers between the substrates, the substrates being made of a material with a dielectric constant having a high rate of decline with frequency;

at least one first capacitor provided on one of the substrates at a first stage area of the connector;

at least one second capacitor provided on one of the substrates at a second stage area of the connector; and

at least one conductive contact provided on the PCB.

35. (Original) The connector of claim 34, wherein the substrate material has a dielectric constant of about 4.0 at 1MHz with a rate of decline being 0.4 per decade of frequency between 1MHz and 1GHz.

36. (Original) The connector of claim 34, wherein the at least one first capacitor includes two first capacitor components formed on at least two of the substrates at the first stage area of the connector.

37. (Original) The connector of claim 36, wherein the two first capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

38. (Original) The connector of claim 34, wherein the at least one second capacitor includes a separate second discreet capacitor surface-mounted on a first one or under a last one of the substrates at the second stage area of the connector.

39. (New) A printed circuit board for providing crosstalk compensation in an electrical connector, comprising:

a plurality of conductive traces;

a first compensation structure providing a first crosstalk compensation signal having a first magnitude to a first of the plurality of conductive traces; and

a second compensation structure providing a second crosstalk compensation signal having a second magnitude to the first of the plurality of conductive traces;

wherein a ratio of the first magnitude to the second magnitude varies with frequency.

40. (New) The printed circuit board of Claim 39, wherein the first compensation structure comprises a capacitor that includes a first dielectric constant material having a first rate of decline with frequency, and wherein the second compensation structure comprises a capacitor that includes a second dielectric constant material having a second rate of decline with frequency, and wherein a difference between the first rate of decline and the second rate of decline is in the range of about 0.15 to about 0.45 per decade of frequency.

41. (New) The printed circuit board of Claim 40, wherein the first rate of decline is about 0.2 per decade of frequency across the frequency range of 1 MHz to 1 GHz.

42. (New) The printed circuit board of Claim 40, wherein the first rate of decline is about 0.4 per decade of frequency across the frequency range of 1 MHz to 1 GHz.

43. (New) The printed circuit board of Claim 40, wherein the second rate of decline is substantially flat with frequency across the frequency range of 1 MHz to 1 GHz.

44. (New) The printed circuit board of Claim 39, wherein the first compensation structure comprises a capacitor that includes a high slope dielectric constant material.

45. (New) The printed circuit board of Claim 43, wherein the second compensation structure comprises a capacitor that includes a low slope dielectric constant material.

46. (New) The printed circuit board of Claim 39, wherein the first crosstalk compensation signal and the second crosstalk compensation signal have different polarities and wherein a time delay is present between the first and second compensation signals.

47. (New) A method of designing an electrical connector, the method comprising:

providing a first compensation signal that varies with frequency at a first rate to a conductor of the electrical connector;

providing a second compensation signal that varies with frequency at a second rate, that is different than the first rate, to the conductor of the electrical connector; and

selecting the first and second rates to reduce the near-end crosstalk on the conductor in the 1 MHz to 100 MHz frequency range when a high crosstalk plug is used in the electrical connector and to reduce the near-end crosstalk on the conductor connector at frequencies above 250 MHz when a low crosstalk plug is used in the electrical connector.

48. (New) The method of Claim 47, wherein providing a first compensation signal that varies with frequency at a first rate comprises providing at least one capacitor in the electrical connector that includes a dielectric constant material having a slope of at least 0.15 per decade of frequency.

49. (New) The printed circuit board of Claim 48, wherein providing a second compensation signal that varies with frequency at a second rate comprises providing at least one capacitor in the electrical connector that includes a dielectric constant material that is substantially flat with frequency.

50. (New) The method of Claim 47, wherein providing a first compensation signal that varies with frequency at a first rate comprises providing a first compensation structure that comprises a capacitor that includes a first dielectric constant material having a first rate of decline with frequency, and wherein providing a second compensation signal that varies with frequency at a second rate comprises providing a second compensation structure that comprises a capacitor that includes a second dielectric constant material having a second rate of decline with frequency, and wherein a difference between the first rate of decline and the second rate of decline is in the range of about 0.15 to about 0.45 per decade of frequency.

51. (New) An electrical connector, comprising:

a plurality of conductive paths that extend from a plurality of respective inputs of the connector to a plurality of respective outputs of the connector;

a first compensation stage for capacitively coupling crosstalk compensation having a first polarity onto a first of the plurality of conductive paths, the first compensation stage including at least one capacitive element that includes a first dielectric constant material that has a first rate of change with frequency; and

a second compensation stage for capacitively coupling crosstalk compensation having a polarity opposite the first polarity onto the first of the plurality of conductive paths, the second compensation stage including at least one capacitive element that includes a second dielectric constant material that has a second rate of change with frequency, wherein the first rate of change and the second rate of change differ by between about 0.15 to about 0.45 per decade of frequency.

52. (New) The electrical connector of Claim 51, wherein the first rate of change is about 0.2 per decade of frequency across the frequency range of 1 MHz to 1 GHz.

53. (New) The electrical connector of Claim 51, wherein the first rate of change is about 0.4 per decade of frequency across the frequency range of 1 MHz to 1 GHz.

54. (New) The electrical connector of Claim 51, wherein the second rate of change is substantially flat with frequency across the frequency range of 1 MHz to 1 GHz.

55. (New) The electrical connector of Claim 51, wherein the first and second rates are pre-selected to reduce the near-end crosstalk on the conductor in the 1 MHz to 100 MHz frequency range when a high crosstalk plug is used in the electrical connector and to reduce the near-end crosstalk on the conductor connector at frequencies above 250 MHz when a low crosstalk plug is used in the electrical connector.

56. (New) A printed circuit board for an electrical connector, the printed circuit board comprising:

a plurality of conductors;

a first capacitor electrically connected to a first of the conductors, the first capacitor having a first dielectric with a first dielectric constant slope; and

a second capacitor electrically connected to the first of the conductors, the second capacitor having a second dielectric with a second dielectric constant slope,

wherein a difference between the first dielectric constant slope and the second dielectric constant slope is at least 0.15 per decade of frequency.

57. (New) The printed circuit board of Claim 56, wherein one of the first dielectric constant slope and the second dielectric constant slope is substantially constant across the frequency range of about 1 MHz to about 1 GHz.

58. (New) A method of designing an electrical connector, the method comprising:

providing a first compensation stage having a first capacitive response as a function of frequency;

providing a second compensation stage having a second capacitive response as a function of frequency;

wherein the first compensation stage and the second compensation stage provide a net compensation, and wherein the first capacitive response as a function of frequency and the second capacitive response as a function of frequency are selected to provide increased net compensation levels at low frequencies and to provide decreased net compensation levels at higher frequencies.